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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,051	03/05/2002	Gerardus Arnoldus Antonius Bos	NL 010979	6456

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
KERVEROS, JAMES C	
ART UNIT	**PAPER NUMBER**
2133	10

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/091,051	Applicant(s) BOS ET AL.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☒ Claim(s) *1-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending and are hereby presented for examination.

Specification

2. The abstract of the disclosure is objected to because of non-compliance with proper language and format. On line 2, the terms "is disclosed" and on line 7, "preferably" should be deleted. Also, the term "e. g" should be avoided. The abstract should be in narrative form and the language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc. Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities:

The specification of the instant application should include the following headings corresponding to the appropriate sections, as provided in 37 CFR 1.77(b). Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

TITLE OF THE INVENTION.

BACKGROUND OF THE INVENTION.

(1) Field of the Invention.

(2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.

BRIEF SUMMARY OF THE INVENTION.

BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).

DETAILED DESCRIPTION OF THE INVENTION.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Appropriate correction is required.

Claim Objections

5. Claims 1-15 are objected to because of the following informalities:

The reference characters enclosed in parenthesis should be deleted from the claims because they do not have patentable weight. Appropriate correction is required.

6. Claims 12 and 13 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 12 is shown to depend from "claim 12" and Claim 13 depend from "claim 13".

Claim 12 should be changed to depend from claim 11 and claim 13 should depend from claim12.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1, 4, 5, 8, 11 and 14 recite the expression "at least partially simultaneous", which renders the claim indefinite, because communication of serial or parallel data in a register cannot occur "partially simultaneous" due to the shift timing requirement. During a serial shift function, the clock shifts the data sequentially where the time duration depends on the number of the clock shift pulses, while in a parallel function, the data is clocked "simultaneous".

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Whetsel (US 6242269).

Regarding independent Claim 1, Whetsel discloses a method for testing a testable electronic device (integrated circuit, 700), FIG. 8, having a first plurality of test arrangements (824-842) and a second plurality of test arrangements (924-942), such as parallel scan paths, comprising:

Serially communicating first test data (serial test data input from a peripheral bond pad 802) between a first shift register (800) and a first test data channel (802), serially communicating second test data (serial test data input from a peripheral bond pad, 902) between a second shift register (900) and a second test data channel (902).

Parallel communicating through parallel inputs (804-822) the first test data (802) between the first plurality of test arrangements (824-842) and the first shift register (800), and also, parallel communicating through parallel inputs (904-922) the second test data (902) between the second plurality of test arrangements (924-942) and the second shift register (900).

Regarding independent Claims 5, 11, Whetsel discloses a testable electronic device (integrated circuit, 700), FIG. 8, comprising:

A first plurality of test arrangements (824-842) and a second plurality of test arrangements (924-942), such as parallel scan paths.

A first contact (802) and a second contact (902), such as bond pads.

A first shift register (800), such as scan distributor coupled between the first contact (802) and the first plurality of test arrangements (824-842) for serially communicating first test data (serial test data input from a peripheral bond pad) with

the first contact (802), and for parallel communicating the first test data through parallel inputs (804-822) with the first plurality of test arrangements (824-842) and

A second shift register (900), such as scan distributor coupled between the second contact (902) and the second plurality of test arrangements (924-942) for serially communicating second test data (serial test data input from a peripheral bond pad) with the second contact (902) at least partially simultaneous with the serial communication of the first test data, and for parallel communicating the second test data through parallel inputs (904-922) with the second plurality of test arrangements (924-942) at least partially simultaneous with the parallel communication of the first test data.

Regarding Claim 2, Whetsel discloses the method steps of copying the first test data (802) from the first shift register (800) into the first buffer register (824-842) and copying the second test data (902) from the second shift register (900) into the second buffer register (924-942), using a testable electronic device (700), wherein the first shift register (800) is coupled to a first buffer register (824-842), and the second shift register (900) is coupled to a second buffer register (924-942).

Regarding Claim 3, Whetsel discloses method steps of:

Serially communicating the first test data channel (802) to the first shift register (800;

Serially communicating the second test data channel (902) to the second shift register (900).

Parallel communicating the first test data (802) from the first shift register (800) to the first plurality of test arrangements (824-842).

Parallel communicating the second test data (1902) from the second shift register (900) to the second plurality of test arrangements (924-942).

Regarding Claim 4, Whetsel discloses method steps of:

Parallel receiving first test result data (846-864) from the first plurality of test arrangements (824-842) in a third shift register (844).

Parallel receiving second test result data (946-964) from the second plurality of test arrangements (924-942) in a fourth shift register (944).

Serially submitting the first test result data from the third shift register (844) to a third test data channel (866).

Serially submitting the second test result data from the fourth shift register (944) to a fourth test data channel (966).

Regarding Claim 6, Whetsel discloses a testable electronic device (700), wherein the first shift register (800) is coupled to the second shift register (900) through MUX 886.

Regarding Claim 7, Whetsel discloses a testable electronic device (700), wherein the first shift register (800) and the second shift register (900) form a boundary scan register.

Regarding Claims 8, 14, Whetsel discloses a testable electronic device (700), wherein the first shift register (800) is arranged to communicate the first test data from the first contact (802) to the first plurality of test arrangements (824-842), and the

second shift register (900) is arranged to communicate the second test data from the second contact (902) to the second plurality of test arrangements (924-942), and wherein the electronic device (700) further comprises:

A third contact (866) and a fourth contact (966);

A third shift register (844) coupled between the third contact (866) and the first plurality of test arrangements (824-842) for serially submitting first test result data to the third contact (206), and for parallel receiving the first test result data (846-864) from the first plurality of test arrangements (824-842).

A fourth shift register (944) coupled between the fourth contact (966) and the second plurality of test arrangements (924-942) for serially submitting second test result data to the fourth contact (966) at least partially simultaneous with the serial submission of the first test result data, and for parallel receiving the second test result data (946-964) from the second plurality of test arrangements (924-942) at least partially simultaneous with the parallel reception of the first test result data.

Regarding Claim 9, Whetsel discloses a testable electronic device (700), wherein the third shift register (844) is coupled to the fourth shift register (944) through DMUX 870.

Regarding Claim 10, Whetsel discloses a testable electronic device (700), wherein the third shift register (844) and the fourth shift register (944) form a boundary scan register.

Regarding Claim 12, Whetsel discloses a testable electronic device (700), wherein the first shift register (800) is coupled to a first buffer register (824-842), and the second shift register (900) is coupled to a second buffer register (924-942).

Regarding Claim 13, Whetsel discloses a testable electronic device (700), wherein the first shift register (800) and the second shift register (900) are responsive to a first clock (CLK1) and the first buffer register (824-842) and the second buffer register (924-942) are responsive to a second clock (CLK2).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel (US 6242269) in view of Giles et al. (US 5812561).

Regarding Claim 15, Whetsel does not explicitly disclose a first plurality of tri-state buffers coupling an output of the first shift register to an input of the third shift register and a second plurality of tri-state buffers coupling an output of the second shift register to an input of the fourth shift register. Whetsel discloses a first buffer register (824-842) coupling a first shift register (880) and a third shift register (844), and a

second buffer register (924-942) coupling a second shift register (900) and a fourth shift register (944).

Giles et al. (US 5812561), in an analogous art, discloses scan based testing of an integrated including a plurality of tri-state buffer drivers (509, 511, 515 and 517) for coupling signal lines 521, 522, 523 and 524. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to deploy the plurality of tri-state buffer drivers as taught by Giles, between the first buffer register (824-842) and the third shift register (844), and also, between the buffer register (924-942) and the fourth shift register (944) of Whetsel, so as to improve fault test coverage and reduces the testing time required for manufactured integrated circuit parts.

Conclusion

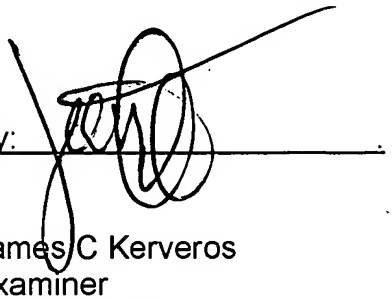
10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 25 June 2004
Office Action: Non-Final Rejection

By: 

James C Kerveros
Examiner
Art Unit 2133

Gregory J. Lamarre for

Albert DeCady
Primary Examiner